REMARKS

Claims 1-18 are pending in the application. Claims 1, 7 and 13 have been amended.

Applicants believe that this response addresses the Examiner's rejection and that any changes do not introduce new matter into the specification, limit the scope of the claims or result in any prosecution history estoppel.

Claim Rejections – 35 USC S. 102

The Examiner stated that the rejections of claims 1-18 under 35 U.S.C. 102(e) as being anticipated by Taubman. Applicants respectfully traverse the Examiner's rejection. In particular, all of the references, either alone or in combination, fail to teach or suggest "determine whether state variables associated with coefficients bits and neighboring bits are zero, wherein a row is read, AND operation is performed to mask out selected bits and zero checked" as claimed or similarly claimed.

Embodiments of the invention reduce the number of instructions it would take for example, to check 18 bits for all zeros. For example, the processor may read row 1 and perform an AND to mask out all but 3 bits, then check for a zero flag. If zero flag, then read the next row, perform an AND, check the zero flag and so on. 2 instructions per row times 6 rows = 12 instructions. As noted in the specification on page 8, paragraph [0034] to page 9, paragraph [0037]:

> [0034] FIG. 4 is a block diagram of an embodiment 400 of register 402 for state variable sigma. In particular, the state variable is shown aligned in a processor's register set. The array of state variable sigmas corresponds to an array of quantized coefficients being scanned. Each bit-plane of a code block is scanned in a particular order. Starting at the top left, the first four bit symbols of the column are scanned. Then the first four bit symbols of the second column, until the width of the code-block has been covered. Then the second four bit symbols of the first column are scanned and so on. A similar scan is continued for any leftover rows on the lowest code blocks in the sub-band. Sigma bits are typically stored in local processors registers in the same scan order as shown in FIG. 4. These can be shifted to the left to perform the same compare on the next scan.
>
> [0035] Embodiments of the instruction will determine whether zero coding or run length coding should be implemented based upon the significance state variable sigmas of selected coefficient bits 404-410 and immediate horizontal and vertical neighboring bits 412-438. If they are zero, then run length coding is performed else zero coding is performed. The instruction is expanded to include NxM zero

checks but in example the zero check is 3X6. This check is preferably performed on every 4 pixels and in every bit plane.

[0036] The zero coding or run length coding decision according to the presently preferred embodiment of the invention may be implemented in response to an instruction set including decision instruction. When implementing this instruction, the host processor controls (either directly or indirectly) the zero coding or run length coding decision. In general, the exact operation sequence to be performed is based on the contents of the block master data structure, which contains the information of the current coefficient block which is being processed. The block master data structure can be implemented in either software or hardware, depending on the embodiment. In the presently preferred embodiments, the block master data structure is implemented as hardware, specifically, as a register set. The registers may include a sigma state variable registers which contains the quantized coefficient values of the stripe currently being scanned and significance values. This register can be connected directly with the memory storage containing the coefficient values, or updated under control of the host processor. During encoding, this register may be scanned to produce the information required to control the operation sequences in the codec.

[0037] In a typical implementation, if the scanning block is 64 pixels by 64 pixels and each pixel is 16 bits, then this check must be performed 64/4 X 64 X 15 = 15360 times. **Embodiments of the invention reduce the number of instruction it would take to check 18 bits for all zeros. With current instructions, the processor typically reads row one and perform an AND to mask out all but 3 bits, then check for a zero flag. If zero flag, then read the next row, perform an AND, check the zero flag and so on. Thus, with two instructions per row times 6 rows = 12 instructions. Embodiments of the invention provide an instruction that is 12 times faster saving 11 X 15360 = 168960 instructions for just a 64 by 64 pixel block. (Emphasis added.)**

Additionally, as noted in the specification on pages 10-11, paragraphs [0043] – [0046]:

[0043] In step 604, state variables associated with horizontal and vertical neighboring bits of the selected bits to be processed are identified.

[0044] In step 606, it is determined whether state variables associated with coefficients bits and neighboring bits are zero.

[0045] In response to state variables associated with coefficient bits and neighboring bits being all zero (step 606), run length coding is selected (step 608).

[0046] In response to at least one state variable associated with coefficient bits and neighboring bits being non-zero (step 606), zero coding is selected (step 610).

In particular, Taubman fails to teach or suggest "determine whether state variables associated with coefficients bits and neighboring bits are zero, wherein a row is read, AND

operation is performed to mask out selected bits and zero checked" as claimed or similarly claimed.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance.

The required fee for a one month extension of time is enclosed. No additional fees are required for additional claims. Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666.

If the Examiner has any questions, he is invited to contact the undersigned at (323) 654-8218. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: December 22, 2005

By _____
Farzad E. Amini, Reg. No. 42,261

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on December 22, 2005.

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Margaux Rodriguez *December 22, 2005*